Page Table Entry

Bit(s)	Field Name	Description
63:48		Reserved
47:16	ADDR	**L2 Entry** Gives the address of a level 3 table. **L3 Entry** Gives bits [47:16] of the output address for a page of memory.
15:11		
10	AF	Access flag. Indicates when a page or section of memory is accessed for the first time.
9:8	SH	Shareability field. 00 : Non-shareable 01 : Reserved 10 : Outer Shareable 11 : Inner Shareable
7:6	AP	Data access permission bits 00 : Kernel Read/Wirte 01 : User Read/Write 10 : Kerenl Read-only 11 : User Read-only
5	NS	Non-secure bit
4:2	ATTR	Memory region attributes 000 : Normal memory 001 : Device memory 010 : Non-cacheable
1	TYPE	**L2 Entry** If 0, the descriptor gives the base address of a *block* of memory, and the attributes for that memory region If 1, the descriptor gives the address of the next level of *translation table*, and some attributes for that translation **L3 Entry** If 0, behaves identically to *invalid* bit[0] set to 0. If 1, gives the address of page of memory
0	VALID	Identifies whether the descriptor is valid. If a lookup returns an invalid descriptor, the associated input address is unmapped, and any attempt to access it generates a translation fault. 0: Invalid 1: Valid